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Stylesheet Version v1.1.1

Claims

[c1] 1. A method for performing power routing on a voltage island within an integrated circuit chip, said method comprising:

generating a first robust power grid for a voltage island on metal levels 1 to N-1;

generating a second robust power grid for said voltage island on metal levels N and above; and

routing a plurality of shortest distance connections from a plurality of power sources to said second robust power grid.

[c2] 2. The method of Claim 1, wherein said second robust power grid is a power segment.

[c3] 3. The method of Claim 1, wherein a number of power segments to be generated on said metal level N and above is determined by determining the product of a number of said power sources and a number of connections to be made per power source.

[c4] 4. The method of Claim 1, wherein said method further includes determining a bounding region of said second robust power grid.

[c5] 5. The method of Claim 1, wherein said generating a second robust power grid further includes:

obtaining a count of power source shapes of an identical voltage polarity on a chip;

identifying a chip position at which said voltage island is located;

determining and generating a bounding region on top of said voltage island on which said routing is to be performed; and

generating power grids within said bounding region.

[c6] 6. The method of Claim 1, wherein said routing further includes:

obtaining a plurality of source points to form an group_A;

dividing said group_A based on connection per source information;

obtaining target power shapes for said second robust power grid on metal level N and above to build a group_B; and

for a given shape s in said group_A, performing shape routing to route from s to a shape t within in said group_B.

[c7] 7. A computer program product residing in a computer storage medium for performing power routing on a volt-

age island within an integrated circuit chip, said computer program product comprising:

program code means for generating a first robust power grid for a voltage island on metal levels 1 to N-1;

program code means for generating a second robust power grid for said voltage island on metal levels N and above;

program code means for determining a bounding region of said second robust power grid; and

program code means for routing a plurality of shortest distance connections from a plurality of power sources to said second robust power grid.

[c8] 8. The computer program product of Claim 7, wherein said second robust power grid is a power segment.

[c9] 9. The computer program product of Claim 7, wherein a number of power segments to be generated on said metal level N and above is determined by determining the product of a number of said power sources and a number of connections to be made per power source.

[c10] 10. The computer program product of Claim 7, wherein said computer program product further includes program code means for determining a bounding region of said second robust power grid.

[c11] 11. The computer program product of Claim 7, wherein said program code means for generating a second robust power grid further includes:

program code means for obtaining a count of power source shapes of an identical voltage polarity on a chip;

program code means for identifying a chip position at which said voltage island is located;

program code means for determining and generating a bounding region on top of said voltage island on which said routing is to be performed; and

program code means for generating power grids within said bounding region.

[c12] 12. The computer program product of Claim 7, wherein said program code means for routing further includes:

program code means for obtaining a plurality of source points to form an group_A;

program code means for dividing said group_A based on connection per source information;

program code means for obtaining target power shapes for said second robust power grid on metal level N and above to build a group_B; and

for a given shape s in said group_A, program code means for performing shape routing to route from s to a shape t in said group_B.

[c13] 13. A computer system for performing power routing on a voltage island within an integrated circuit chip, said computer system comprising:

means for generating a first robust power grid for a voltage island on metal levels 1 to N-1;

means for generating a second robust power grid for said voltage island on metal levels N and above;

means for determining a bounding region of said second robust power grid; and

means for routing a plurality of shortest distance connections from a plurality of power sources to said second robust power grid.

[c14] 14. The computer system of Claim 13, wherein said second robust power grid is a power segment.

[c15] 15. The computer system of Claim 13, wherein a number of power segments to be generated on said metal level N and above is determined by determining the product of a number of said power sources and a number of connections to be made per power source.

[c16] 16. The computer system of Claim 13, wherein said computer system further includes means for determining a bounding region of said second robust power grid.

[c17] 17. The computer system of Claim 13, wherein said

means for generating a first robust power grid further includes:

means for obtaining a count of power source shapes of an identical voltage polarity on a chip;

means for identifying a chip position at which said voltage island is located;

means for determining and generating a bounding region on top of said voltage island on which said routing is to be performed; and

means for generating power grids within said bounding region.

[c18] 18. The computer system of Claim 13, wherein said means for routing further includes:

means for obtaining a plurality of source points to form an group_A;

means for dividing said group_A based on connection per source information;

means for obtaining target power shapes for said second robust power grid on metal level N and above to build a group_B; and

for a given shape s in said group_A, means for performing shape routing to route from s to a shape t in said group_B.

[c19] 19. A method for performing power routing on a voltage island within an integrated circuit chip, said method

comprising:

generating a set of power segments to provide a robust power grid for a voltage island;

determining a bounding region of said robust power grid; and

routing a plurality of shortest distance connections from a plurality of power sources to said robust power grid.

[c20] 20. The method of Claim 19, wherein said number of power segments is determined by determining the product of a number of said power sources and a number of connections to be made per power source.

[c21] 21. The method of Claim 19, wherein said routing further includes:

obtaining a count of power source shapes of an identical voltage polarity on a chip;

identifying a chip position at which said voltage island is located;

determining and generating a bounding region on top of said voltage island on which said routing is to be performed; and

generating power grids within said bounding region.